Notice of Allowability	Application No.	Applicant(s)	
	09/628,705	CHAKRAVORTY, KISHORE K.	
	Examiner	Art Unit	
	Tuan T. Dinh	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *04/27/05*.

2. ☒ The allowed claim(s) is/are *1-2,6-8,12-14,16-18,32-40,42-45 (renumber claims are 1-24)*.

3. ☒ The drawings filed on *31 July 2000* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 02/07/05
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Walt Nielsen (Reg. No. 25,539) on April 27, 2005.

The application has been amended as follows: to overcome the references cited.

Cancel claims 10-11, 31, and 41 without prejudice.

Claims 1, 12, and 16 should be amended as below:

For claim 1:

(Twice Currently Amended) An interposer to couple a die to a substrate and comprising:

a plurality of power and ground vias in a core region of the interposer;

a plurality of signal vias in a peripheral region of the interposer;

an embedded capacitor having first and second terminals;

a first surface including a first plurality of power lands coupled to the first terminal through first ones of the plurality of power vias and a first plurality of ground lands coupled to the second terminal through first ones of the plurality of ground vias and

a second surface including a second plurality of power lands coupled to the first terminal through second ones of the plurality of power vias and a second plurality of ground lands coupled to the second terminal through second ones of the plurality of ground vias;

wherein the first plurality of power lands and the first plurality of ground lands are positioned to be coupled to corresponding power and ground nodes of the die through controlled collapse chip connect solder bumps;

wherein the first surface comprises a first plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the die; and

wherein the second surface comprises a second plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the substrate.

For claim 12:

(Twice Currently Amended) An electronic assembly comprising:

a die comprising a first plurality of power nodes and a first plurality of ground nodes;

a substrate comprising a second plurality of power nodes and a second plurality of ground nodes: and

an interposer coupling the die to the substrate and including a plurality of power and ground vias in a core region of the interposer;

a plurality of signal vias in a peripheral region of the interposer;

an embedded capacitor having a first terminal and a second terminal;

a first surface including a first plurality of power lands coupled to the first terminal through first ones of the plurality of power vias, and a first plurality of ground lands coupled to the second terminal through first ones of the plurality of ground vias: and

a second surface including a second plurality of power lands coupled to the first terminal through second ones of the plurality of power vias, and a second plurality of mound lands coupled to the second terminal through second ones of the plurality of mound vias;

wherein the first plurality of power lands and the first plurality of ground lands are coupled to the respective first plurality of power nodes and first plurality of ground nodes of the die, and

wherein the second plurality of power lands and the second plurality of ground lands are coupled to the respective second plurality of power nodes and second plurality of ground nodes of the substrate;

wherein the first surface comprises a first plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the die; and

wherein the second surface comprises a second plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the substrate.

For claim 16:

(Twice Currently Amended) An electronic system comprising an electronic assembly comprising:

a die comprising a first plurality of power nodes and a first plurality of ground nodes;

a substrate comprising a second plurality of power nodes and a second plurality of ground nodes, and

an interposer coupling the die to the substrate and including

a plurality of power and ground vias in a core region of the interposer;

a plurality of signal vias in a peripheral region of the interposer;

an embedded capacitor having a first terminal and a second terminal

a first surface including a first plurality of power lands coupled to the first terminal through first ones of the plurality of power vias, and a first plurality of around lands coupled to the second terminal through first ones of the plurality of ground vias, and

a second surface including a second plurality of power lands coupled to the first terminal through second ones of the plurality of power vias, and a second plurality of ground lands coupled to the second terminal through second ones of the plurality of ground vias;

wherein the first plurality of power lands and the first plurality of ground lands are coupled to the respective first plurality of power nodes and first plurality of mound nodes of the die: and

wherein the second plurality of power lands and the second plurality of ground lands are coupled to the respective second plurality of power nodes and second plurality of ground nodes of the substrate

wherein the first surface comprises a first plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the die; and

wherein the second surface comprises a second plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the substrate.

Allowable Subject Matter

2. Claims 1-2, 6-8, 12-14, 16-18, 32-40, and 42-45 are allowed (renumber claims are 1-24).

The following is an examiner's statement of reasons for allowance: the references cited disclose an interposer, an electronic assembly, and an electronic system comprising a plurality of power, ground, and signal vias, an embedded capacitor, first and second surfaces including first and second plurality of power and ground lands, and some other claimed elements. However, they do not disclose or render obvious in combination of the first surface comprises a first plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the die; and the second surface comprises a second

plurality of signal lands coupled to the plurality of signal vias and positioned to be coupled to corresponding signal nodes of the substrate.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hale et al. and Figueroa et al disclose related art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Dinh
April 27, 2005.

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800